CLAIMS IN THE CASE

Please cancel Claims 1-36, without prejudice.

Please add new Claims 37-78.

1- 36. (Cancelled)

37. (New) A method of scheduling and executing instructions comprising:

a) accessing a sequence of instructions comprising:

a first memory operation that involves a first address range;

a second memory operation that involves at least a portion of said first address range; and

a third memory operation intervening said first and second memory operations, wherein it is not known whether said third memory operation involves an address within said first address range, wherein at least one of said first through third memory operations comprises a store operation;

b) eliminating said second memory operation from said sequence of instructions;

c) executing said sequence of instructions with said second memory operation eliminated; and

d) determining, during said executing, if said third memory operation involves an address within said first address range.

38. (New)The method of Claim 37, further comprising, prior to said executing said sequence of instructions, adding information to said third memory operation to allow determination of said first address range.

39. (New) The method of Claim 38, wherein said information comprises a mask allowing determination of which of a plurality of registers hold protected addresses.

40. (New) The method of Claim 39, wherein said d) further comprises determining, during said executing, if said third memory operation involves an address within a range of any of said protected addresses.

41. (New) The method of Claim 39, further comprising storing a memory address associated with said first address range in one of said plurality of registers prior to said executing said sequence of instructions.

42. (New) The method of Claim 37, further comprising storing a memory address associated with said first address range in a register prior to said executing said sequence of instructions.

43. (New) The method of Claim 42, wherein:

said sequence of instruction comprises a fourth memory operation that is in said sequence of instructions after said first memory operation; and

further comprising adding information to said fourth memory operation that allows said fourth memory operation to execute without exception even if said fourth memory operation involves said first address range.

44. (New) The method of Claim 37, wherein said first and second memory operations would be safely reducible to a single memory operation if said third memory operation were not intervening.

45. (New) A method of scheduling and executing instructions comprising:

a) accessing a sequence of instructions comprising:

a first load instruction that loads from a first address range;

a second load instruction that loads from said first address range; and

a store instruction intervening said first and second load instructions, wherein it is not known whether said store instruction stores to an address within said first address range;

b) eliminating said second load instruction from said sequence of instructions;

c) executing said sequence of instructions without said second load instruction; and

d) determining, during said execution, if said store instruction stores to an address within said first address range.

46. (New) The method of Claim 45, wherein said b) further comprises storing a memory address associated with said first address range in a protection register.

47. (New) The method of Claim 46, wherein said b) further comprises adding a flag to said store instruction to indicate said protection register.

48. (New) The method of Claim 45, wherein said b) further comprises changing said first load instruction to a load and protect instruction.

49. (New) A method of scheduling and executing instructions comprising:

a) accessing a sequence of instructions comprising:

a first store instruction to a first address range;

a second store instruction to said first address range; and

a load instruction intervening said first and second store instructions, wherein it is not known whether said load instruction involves said first address range;

b) eliminating said first store instruction from said sequence of instructions;

c) executing said sequence of instructions with said first stored instruction removed; and

d) determining, during said executing, if said load instruction involves an address in said first address range.

50. (New) The method of Claim 49, wherein said b) further comprises storing a memory address associated with said load instruction in a protection register.

51. (New) The method of Claim 50, wherein said b) further comprises adding a flag to said second store instruction to indicate said protection register.

52. (New) The method of Claim 49, wherein said b) further comprises changing said load instruction to a load and protect instruction.

53. (New) A method of scheduling and executing instructions comprising:

a) accessing a sequence of instructions comprising:

a store instruction;

a load instruction to a first address range and following said store instruction in said sequence of instructions, wherein it is not known whether said store instruction involves said first address range;

b) placing said load instruction prior to said store instruction in said sequence of instructions;

c) executing said sequence of instructions after placing said load instruction prior to said store instruction; and

d) determining, during said executing, if said store instruction involves an address in said first address range.

54. (New) The method of Claim 53, wherein said b) further comprises storing an address range of memory accessed by said load instruction in a protection register.

55. (New) The method of Claim 54, further comprising adding a flag to said store instruction to indicate said protection register.

56. (New) The method of Claim 53, wherein said b) further comprises changing said load instruction to a load and protect instruction.

57. (New) A method of scheduling and executing instructions comprising:

a) accessing a sequence of instructions comprising:

a load instruction;

a store instruction to a first address range and following said load instruction in said sequence of instructions, wherein it is not known whether said load instruction involves said first address range;

b) placing said store instruction prior to said load instruction in said sequence of instructions;

c) executing said sequence of instructions after placing said store instruction prior to said load instruction in said sequence of instructions; and

d) determining, during said executing, if said load instruction involves an address in said first address range.

58. (New) The method of Claim 57, wherein said b) further comprises storing an address range of memory accessed by said store instruction in a protection register.

59. (New) The method of Claim 58, further comprising adding a flag to said load instruction to indicate said protection register.

60. (New) The method of Claim 57, wherein said b) further comprises changing said store instruction to a store and protect instruction.

61. (New) A method of scheduling and executing instructions comprising:

a) accessing a sequence of instructions comprising:

a first store instruction;

a second store to a first address range and following said first store instruction in said sequence of instructions, wherein it is not known whether said first store instruction involves said first address range;

b) placing said second store instruction prior to said first store instruction in said sequence of instruction;

c) executing said sequence of instructions after placing said second store instruction prior to said first store instruction in said sequence of instruction; and

d) determining, during said execution, if said first store instruction involves an address in said first address range.

62. (New) The method of Claim 61, wherein said b) further comprises changing said second store instruction to a store and protect instruction to protect data stored by said second store instruction from being overwritten due to moving said second store instruction in said sequence of instructions.

63. (New) The method of Claim 61, wherein said b) further comprises storing an address range where data is stored by said second store instruction in a protection register.

64. (New) The method of Claim 63, further comprising adding a flag to said first store instruction to indicate said protection register.

65. (New) A method of scheduling and executing instructions comprising:

a) accessing a sequence of instructions comprising:

a loop of instructions comprising:

a first memory operation involving a first address range; and

a second memory operation, wherein it is not known whether said second memory operation involves said first address range, and wherein at least one of said first and second memory operations comprises a store instruction;

b) removing said first memory operation from said loop of instructions;

c) executing said sequence of instructions after said removal; and

d) determining, during said execution, if involves said second memory operation involves first address range.

66. (New) The method of Claim 65, further comprising adding a flag to said second memory operation to indicate a register containing a protected address prior to said executing said sequence of instructions.

67. (New) The method of Claim 65, further comprising storing a memory address associated with said first address range in said register prior to said executing said sequence of instructions.

68. (New) The method of Claim 65, wherein said first memory operation comprises a load operation.

69. (New) The method of Claim 65, wherein said second memory operation comprises a load operation.

70. (New) The method of Claim 65, wherein said second memory operation comprises a store operation.

71. (New) A method of scheduling and executing instructions comprising:

a) accessing a sequence of instructions comprising:

a first store instruction that stores to a first address range;

a load instruction that loads from said first address range; and

a second store instruction intervening said first store instruction and said load instruction, wherein it is not known whether said second store instruction stores to an address within said first address range;

b) eliminating said load instruction from said sequence of instructions;

c) executing said sequence of instructions without said load instruction; and

d) determining, during said execution, if said second store instruction stores to an address within said first address range.

72. (New) The method of Claim 71, wherein said b) further comprises storing a memory address associated with said first address range in a protection register.

73. (New) The method of Claim 72, wherein said b) further comprises adding a flag to said second store instruction to indicate said protection register.

74. (New) The method of Claim 71, wherein said b) further comprises changing said first store instruction to a store and protect instruction.

75. (New) A method of scheduling and executing instructions comprising:

a) accessing a sequence of instructions comprising:

a load instruction that loads from a first address range;

a first store instruction, wherein it is not known whether said first store instruction stores to an address within said first address range;

a second store that stores to said first address range, wherein said first store instruction intervenes said load instruction and said second store instruction;

b) eliminating said second store instruction from said sequence of instructions;

c) executing said sequence of instructions without said second store instruction; and

d) determining, during said execution, if said first store instruction stores to an address within said first address range.

76. (New) The method of Claim 75, wherein said b) further comprises storing a memory address associated with said first address range in a protection register.

77. (New) The method of Claim 76, wherein said b) further comprises adding a flag to said first store instruction to indicate said protection register.

78. (New) The method of Claim 75, wherein said b) further comprises changing said load instruction to a load and protect instruction.